Synchronous Ethernet

In This Chapter

This section provides information about Synchronous Ethernet (SyncE).

Topics in this section include:

Applicability

This example is applicable to all of the 7750 SR, 7710 SR and 7450 ESS series, except for the SR-1 and ESS-1, and was tested on release 8.0r7. There are no software pre-requisites for this configuration, however, the hardware requires the use of Synchronous Ethernet capable MDA-XPs/CMA-XPs or the IMMs.

In addition, Synchronous Ethernet is only supported on optical interfaces. It is not supported on 10/100/1000 base copper interfaces.

Summary

Synchronous Ethernet (SyncE) is the ability to provide PHY-level frequency distribution through an Ethernet port. It is one of the building blocks of Next Generation Networks (NGNs).

Overview

Synchronous Ethernet

Traditionally, Ethernet based networks employ the physical layer transmitter clock to be derived from an inexpensive +/-100ppm crystal oscillator and the receiver locks onto it. There is no need for long term frequency stability as the data is packetized and can be buffered. For the same reason there is no need for consistency between the frequencies of different links. However one could elect to derive the physical layer transmitter clock from a high quality frequency reference by replacing the crystal with a frequency source traceable to a primary reference clock. This would not affect the operation of any of the Ethernet layers, for which this change would be transparent. The receiver at the far end of the link would lock onto the physical layer clock of the received signal, and thus itself gain access to a highly accurate and stable frequency reference. Then, in a manner analogous to conventional hierarchical master-slave network synchronization, this receiver could lock the transmission clock of its other ports to this frequency reference and a fully time synchronous network could be established.

The advantage of using SyncE, as compared to methods relying on sending timing information in packets over an unlocked physical layer, is that SyncE is not influenced by impairments introduced by the higher levels of the networking technology (packet loss, packet delay variation). Hence, the frequency accuracy and stability may be expected to exceed those of networks with unsynchronized physical layers. In addition, SyncE was designed to integrate into any existing SONET/SDH synchronization distribution architecture to allow for the easy migration from the traditional to the new synchronous interfaces. SyncE includes the concept of a Hybrid Switch which supports the interworking of synchronization distribution through SONET/SDH and the SyncE interfaces at the same time.

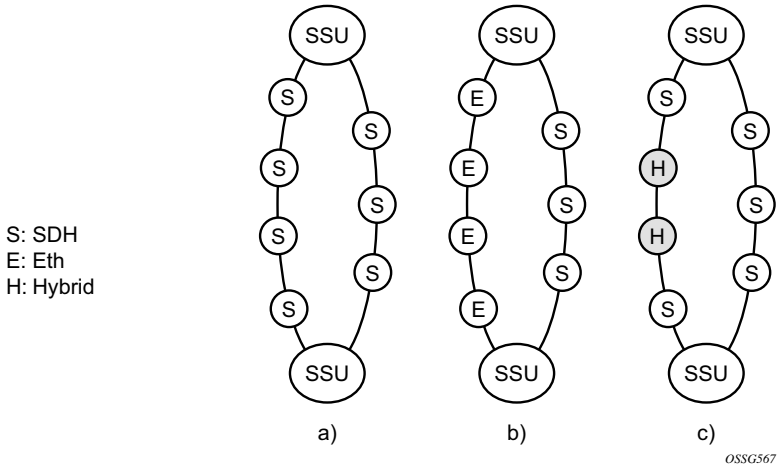

Figure 1: SyncE Hypothetical Reference Network Architecture

Many Tier 1 carriers are looking to migrate their synchronization infrastructure to a familiar and manageable model. In order to enable rapid migration of these networks, SyncE may be the easiest to deploy in order to ensure robust frequency synchronization.

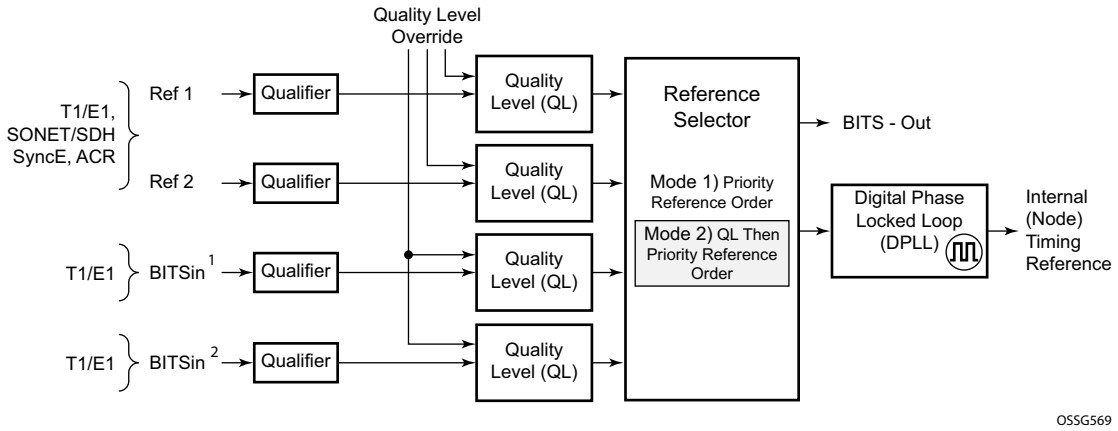

Figure 2: Packet Based Network Timing Infrastructure

Central Synchronization Sub-System

The timing subsystem for the SR/ESS platforms has a central clock located on the Control Processor Module (CPM). The timing subsystem performs many of the duties of the network element clock as defined by Telcordia (GR-1244) and ITU-T G.781.

The system can select from up to four timing inputs to train the local oscillator. The priority order of these references must be specified. This is a simple ordered list of inputs: {BITS [Building Integrated Timing Source], ref1, ref2}. The CPM clock output has the ability to drive the clocking for all line cards in the system. The SR/ESS supports selection of the node reference using Quality Level (QL) indications.

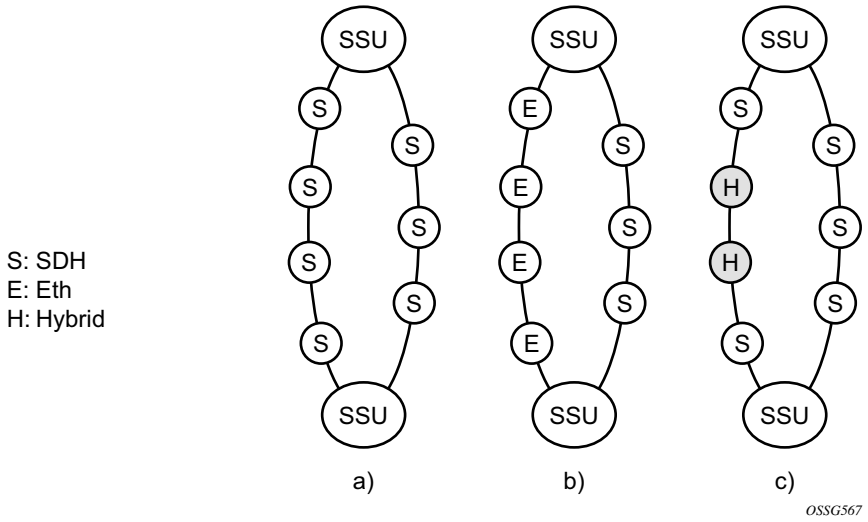

Figure 3: Current 7x50 Timing Sub-System Architecture

[1] BITSin port on Active CPM (7750 SR-7/12, 7450 ESS-7/12) or BITS_1 port on 7750 SR-c4.

[2] BITSin port on Standby CPM (7750 SR-7/12, 7450 ESS-7/12) or BITS_2 port on 7750 SR-c4.

The recovered clock is able to derive its timing from any of the following:

- OC3/STM1, OC12/STM4, OC48/STM16, OC192/STM64 ports
- T1/E1 CES channel (adaptive clocking)
- SyncE ports
- T1/E1 ports
- BITS port on a Channelized OC3/STM1 CES CMA (7710 SR-c4, 7710 SR-c12, and the 7750 SR-c12)
- BITS port on the CPM or CFM module

On 7750 SR-12 and 7750 SR-7 systems with redundant CPMs, the system has two BITS input ports (one per CPM). On the 7750 SRc-4 systems, there are two BITS input ports on the chassis front plate. These BITS input ports provide redundant synchronization inputs from an external BITS/SSU. Note the 7750 SR-c12 does not support BITS input port redundancy or BITS out.

All settings of the signal characteristics for the BITS input apply to both ports. When the active CPM considers the BITS input as a possible reference, it will consider first the BITS input port on the active CPM followed the BITS input port on the standby CPM in that relative priority order. This relative priority order is in addition to the user definable ref-order. For example, a ref-order of ‘bits-ref1-ref2’ would actually be BITS in (active CPM) followed by BITS in (standby CPM)

followed by ref1 followed by ref2. When ql-selection is enabled, then the QL of each BITS input port is viewed independently. The higher QL source is chosen.

On the 7750 SR-c4 platform CFM, there are two BITS input ports and two BITS output ports on this one module. These two ports are provided for BITS redundancy for the chassis. All settings of the signal characteristics for the BITS input apply to both ports. This includes the ql-override setting. When the CFM considers the BITS input as a possible reference, it will consider first the BITS input port “bits1” followed the BITS input port “bits2” in that relative priority order. This relative priority order is in addition to the user definable ref-order. For example, a ref-order of ‘bits-ref1-ref2’ would actually be “bits1” followed by “bits2” followed by ref1 followed by ref2. When ql-selection is enabled, then the QL of each BITS input port is viewed independently. The higher QL source is chosen.

The BITS output ports are provided to deliver a unfiltered recovered line clock from a SR/ESS port directly to a dedicated timing device in the facility (BITS or Standalone Synchronization Equipment (SASE) device). The signal selected will be one of ref1 or ref2. It cannot be the BITS input port signal nor can it be the output of the central clock.

When QL selection mode is disabled, then the reversion setting controls when the central clock can re-select a previously failed reference.

Table 1: Revertive, Non-Revertive Timing Reference Switching Operation

Status of Reference A	Status of Reference B	Active Reference Non-revertive Case	Active Reference Revertive Case
OK	OK	A	A
Failed	OK	B	B
OK	OK	B	A
OK	Failed	A	A
OK	OK	A	A
Failed	Failed	holdover	holdover
OK	Failed	A	A
Failed	Failed	holdover	holdover
Failed	OK	B	B
Failed	Failed	holdover	holdover
OK	OK	A or B	A

Synchronization Status Messages (SSM)

SSM provides a mechanism to allow the synchronization distribution network to both determine the quality level of the clock sourcing a given synchronisation trail and to allow a network element to select the best of multiple input synchronization trails. Synchronization Status messages have been defined for various transport protocols including SONET/SDH, T1/E1, and SyncE, for interaction with office clocks, such as BITS or SSUs (synchronisation supply unit) and embedded network element clocks.

SSM allows equipment to autonomously provision and reconfigure (by reference switching) their synchronization references, while helping to avoid the creation of timing loops. These messages are particularly useful to allow synchronization reconfigurations when timing is distributed in both directions around a ring.

In SyncE, the SSM is provided through the Ethernet Synchronization Messaging Channel (ESMC). This mechanism uses Ethernet OAM PDU to exchange the Quality Level values over the SyncE link.

SyncE Chains

Transmission of a reference clock through a chain of Ethernet equipment requires that all of the equipment support SyncE.

A single piece of equipment not capable of SyncE breaks the chain as shown in Figure 4. Ethernet frames will still get through but downstream device will recognize that the signal is out of pull-in range and not use it for reference.

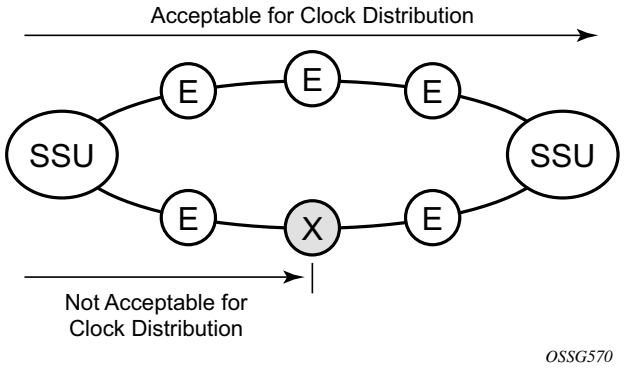

Figure 4: Network Considerations for Ethernet Timing Distribution

Configuration

Configuration 1

The following example shows the configuration options for SyncE when ql-selection mode is disabled. Generally, North American SONET networks do not use the automatic reference selection mechanisms. If SyncE is being added into such a network it would likely have ql-selection set to disabled.

```
A:PE-1>config# card 1 mda 1
A:PE-1>config>card>mda#
     access          + Configure access MDA parameters
     egress          + Configure egress MDA parameters
[no] hi-bw-mcast-src - Enable/disable allocation of resources for high
                       bandwidth multicast streams
     ingress         + Configure ingress MDA parameters
[no] mda-type        - Provisions/de-provisions an MDA to/from the device
                       configuration for the slot
     named-pool-mode + Enable/Disable named pool mode
     network         + Configure network MDA parameters
[no] shutdown        - Administratively shut down an mda
[no] sync-e          - Enable/Disable Synchronous Ethernet
A:PE-1>config>card>mda# sync-e
*A:PE-1>config>card>mda# info detail
----------------------------------------------
           mda-type m20-1gb-xp-sfp
           sync-e
           named-pool-mode
               ingress
                   no named-pool-policy
               exit
               egress
                   no named-pool-policy
               exit
           exit
           ingress
               no hsmda-pool-policy
               no scheduler-policy
           exit
           egress
               no hsmda-pool-policy
           exit
           network
               ingress
                   pool default
          ...
```

```
*A:PE-1>config>system# sync-if-timing
*A:PE-1>config>system>sync-if-timing#
      abort           - Discard the changes that have been made to sync
                        interface timing during a session
      begin           - Switch to edit mode for sync interface timing - use
                        commit to save or abort to discard the changes made in
                        a session
      bits            + Configure parameters for the Building Integrated Timing
                        Supply(BITS)
      commit          - Save the changes made to sync interface timing during a
                        session
 [no] ql-selection    - Enable/disable reference selection based on
                        quality-level
 [no] ref-order       - Priority order of timing references
      ref1            + Configure parameters for the first timing reference
      ref2            + Configure parameters for the second timing reference
 [no] revert          - Revert/do not revert to a higher priority re-validated
                        reference source
*A:PE-1>config>system>sync-if-timing# begin
*A:PE-1>config>system>sync-if-timing# ref-order bits ref1
*A:PE-1>config>system>sync-if-timing# bits input no shutdown
*A:PE-1>config>system>sync-if-timing# bits interface-type ds1 esf
*A:PE-1>config>system>sync-if-timing# revert
*A:PE-1>config>system>sync-if-timing# ref1
*A:PE-1>config>system>sync-if-timing>ref1#
 [no] ql-override     - Override the quality level of a timing reference
 [no] shutdown        - Administratively shutdown the timing reference
 [no] source-port     - Configure the source port for the first timing reference
*A:PE-1>config>system>sync-if-timing>ref1# source-port 1/1/2
*A:PE-1>config>system>sync-if-timing>ref1# no shutdown
*A:PE-1>config>system>sync-if-timing>ref1# exit
*A:PE-1>config>system>sync-if-timing# commit
*A:PE-1>config>system>sync-if-timing# info detail
----------------------------------------------
            no ql-selection
            ref-order bits ref1 ref2
            ref1
                source-port 1/1/2
                no shutdown
                no ql-override
            exit
            ref2
                shutdown
                no source-port
                no ql-override
            exit
            bits
                interface-type ds1 esf
                no ql-override
                input
                    no shutdown
                exit
                output
                    shutdown
                    line-length 110
                exit
            exit
            revert
```

The following output displays the associated show information.

```
*A:PE-1>show>system# sync-if-timing
===============================================================================
System Interface Timing Operational Info
===============================================================================
System Status CPM A                : Master Locked
    Reference Input Mode           : Revertive
    Quality Level Selection        : Disabled
    Reference Selected             : ref1
    System Quality Level           : unknown
    Current Frequency Offset (ppm) : -5

Reference Order                    : bits ref1 ref2

Reference Mate CPM
    Qualified For Use              : No
        Not Qualified Due To       :     LOS
    Selected For Use               : No
        Not Selected Due To        :     not qualified

Reference Input 1
    Admin Status                   : up
    Rx Quality Level               : unknown
    Quality Level Override         : none
    Qualified For Use              : Yes
    Selected For Use               : Yes
    Source Port                    : 1/1/2

Reference Input 2
    Admin Status                   : down
    Rx Quality Level               : unknown
    Quality Level Override         : none
    Qualified For Use              : No
        Not Qualified Due To       :     disabled
    Selected For Use               : No
        Not Selected Due To        :     disabled
    Source Port                    : None

Reference BITS A
    Input Admin Status             : up
    Rx Quality Level               : failed
    Quality Level Override         : none
    Qualified For Use              : No
        Not Qualified Due To       :     LOS
    Selected For Use               : No
        Not Selected Due To        :     not qualified
    Interface Type                 : DS1
    Framing                        : ESF
    Line Coding                    : B8ZS
===============================================================================
*A:PE-1>show>system#
```

Configuration 2

The following example shows the configuration options for SyncE when ql-selection mode is enabled.

This is the normal case for European SDH networks.

```
A:PE-1>config# card 1 mda 1
A:PE-1>config>card>mda#
     access          + Configure access MDA parameters
     egress          + Configure egress MDA parameters
[no] hi-bw-mcast-src - Enable/disable allocation of resources for high
                       bandwidth multicast streams
     ingress         + Configure ingress MDA parameters
[no] mda-type        - Provisions/de-provisions an MDA to/from the device
                       configuration for the slot
     named-pool-mode + Enable/Disable named pool mode
     network         + Configure network MDA parameters
[no] shutdown        - Administratively shut down an mda
[no] sync-e          - Enable/Disable Synchronous Ethernet
A:PE-1>config>card>mda# sync-e
A:PE-1>config>card>mda# info detail
----------------------------------------------
           mda-type m20-1gb-xp-sfp
           sync-e
           named-pool-mode
               ingress
                   no named-pool-policy
               exit
               egress
                   no named-pool-policy
               exit
           exit
           ingress
               no hsmda-pool-policy
               no scheduler-policy
           exit
           egress
               no hsmda-pool-policy
           exit
           network
               ingress
                   pool default
          ...


A:PE-1>config# port 1/1/2 ethernet ssm
A:PE-1>config>port>ethernet>ssm#
A:PE-1>config>port>ethernet>ssm#
 [no] code-type       - Set the SSM channel to either use sonet or sdh
 [no] shutdown        - Enable/Disable SSM
 [no] tx-dus          - Enable/disable always transmit 0xF (dus/dnu) in SSM messaging chan-
nel

A:PE-1>config>port>ethernet>ssm# code-type sdh
*A:PE-1>config>port>ethernet>ssm# no shutdown
*A:PE-1>config>port>ethernet>ssm# info detail
```

```
-----------------------------------------------
                code-type sdh
                no tx-dus
                no shutdown
-----------------------------------------------
*A:PE-1>config>port>ethernet>ssm#



*A:PE-1>config>system# sync-if-timing
*A:PE-1>config>system>sync-if-timing#
      abort           - Discard the changes that have been made to sync
                        interface timing during a session
      begin           - Switch to edit mode for sync interface timing - use
                        commit to save or abort to discard the changes made in
                        a session
      bits            + Configure parameters for the Building Integrated Timing
                        Supply(BITS)
      commit          - Save the changes made to sync interface timing during a
                        session
 [no] ql-selection    - Enable/disable reference selection based on
                        quality-level
 [no] ref-order       - Priority order of timing references
      ref1            + Configure parameters for the first timing reference
      ref2            + Configure parameters for the second timing reference
 [no] revert          - Revert/do not revert to a higher priority re-validated
                        reference source
*A:PE-1>config>system>sync-if-timing# begin
*A:PE-1>config>system>sync-if-timing# ref-order bits ref1
*A:PE-1>config>system>sync-if-timing# ql-selection
*A:PE-1>config>system>sync-if-timing# bits input no shutdown
*A:PE-1>config>system>sync-if-timing# bits interface-type ds1 esf
*A:PE-1>config>system>sync-if-timing# bits ql-override prc
*A:PE-1>config>system>sync-if-timing# revert
*A:PE-1>config>system>sync-if-timing# ref1
*A:PE-1>config>system>sync-if-timing>ref1#
 [no] ql-override     - Override the quality level of a timing reference
 [no] shutdown        - Administratively shutdown the timing reference
 [no] source-port     - Configure the source port for the first timing reference
*A:PE-1>config>system>sync-if-timing>ref1# source-port 1/1/2
*A:PE-1>config>system>sync-if-timing>ref1# no shutdown
*A:PE-1>config>system>sync-if-timing>ref1# exit
*A:PE-1>config>system>sync-if-timing# commit
*A:PE-1>config>system>sync-if-timing# info detail
-----------------------------------------------
            ql-selection
            ref-order bits ref1 ref2
            ref1
                source-port 1/1/2
                no shutdown
                no ql-override
            exit
            ref2
                shutdown
                no source-port
                no ql-override
            exit
            bits
                interface-type ds1 esf
```

```
            ql-override prc
            input
                no shutdown
            exit
            output
                shutdown
                line-length 110
            exit
        exit
        revert
```

The following output displays the associated show information.

```
*A:PE-1>show>system# sync-if-timing
===============================================================================
System Interface Timing Operational Info
===============================================================================
System Status CPM A                : Master Locked
    Reference Input Mode           : Revertive
    Quality Level Selection        : Enabled
    Reference Selected             : ref1
    System Quality Level           : prc
    Current Frequency Offset (ppm) : -5

Reference Order                    : bits ref1 ref2

Reference Mate CPM
    Qualified For Use              : No
        Not Qualified Due To       :     LOS
    Selected For Use               : No
        Not Selected Due To        :     not qualified

Reference Input 1
    Admin Status                   : up
    Rx Quality Level               : prc
    Quality Level Override         : none
    Qualified For Use              : Yes
    Selected For Use               : Yes
    Source Port                    : 1/1/2

Reference Input 2
    Admin Status                   : down
    Rx Quality Level               : unknown
    Quality Level Override         : none
    Qualified For Use              : No
        Not Qualified Due To       :     disabled
    Selected For Use               : No
        Not Selected Due To        :     disabled
    Source Port                    : None

Reference BITS A
    Input Admin Status             : up
    Rx Quality Level               : failed
    Quality Level Override         : none
    Qualified For Use              : No
        Not Qualified Due To       :     LOS
    Selected For Use               : No
        Not Selected Due To        :     not qualified
```

```
    Interface Type                : DS1
    Framing                       : ESF
    Line Coding                   : B8ZS
===============================================================================
*A:PE-1>show>system#
```

Conclusion

With the world rapidly transitioning to IP/MPLS-based NGNs with Ethernet as the transport medium of choice, there is an increasing need to enhance services and capabilities while still leveraging existing infrastructure, thereby easing the transition while continuing to increase revenue and reduce the Total Cost of Ownership (TCO). In areas such as mobile backhaul, TDM CES etc., these requirements create a need for SONET/SDH-like frequency synchronization capability in the inherently asynchronous Ethernet network.

SyncE, natively supported on the Alcatel-Lucent 7750 SR and 7450 ESS service routers, is an ITU-T standardized PHY-level way of transmitting frequency synchronization across Ethernet packet networks that fulfills that need in a reliable, secure, scalable, efficient, and cost-effective manner. It allows Service Providers to keep existing revenue streams alive and create new ones while simplifying the network design and reducing TCO.